PVP 14

Code: IT3T1

II B.Tech - I Semester – Regular Examinations – December 2015

DIGITAL SYSTEM DESIGN
(INFORMATION TECHNOLOGY)

Duration: 3 hours Max. Marks: 70

PART – A

Answer ***all*** the questions. All questions carry equal marks

11x 2 = 22 M

1. a) In how many ways we can represent negative number and what are they?
   b) Who invented k-map and what is the other name for karnaugh map?
   c) Draw the block diagram of ROM.
   d) What are AOI GATES?
   e) In how many ways we can represent NOR gate what they are?
   f) Draw the block diagram of synchronous and asynchronous sequential logic.
   g) What are even and odd functions?
   h) What is register transfer logic?
   i) What are the symbols used to represent SOP, POS, don't care and invert?
   j) Write the difference between prime implicants and essential prime implicants.
   k) Draw the block diagrams of half subtractor and full subtractor.

PART – B

Answer any ***THREE*** questions. All questions carry equal marks. 3 x 16 = 48 M

2. a) Determine the base of the numbers in each case for the following operations to be correct: 8 M

i) 14/2 = 5 ii) 54/4=13 iii) 24+17=40

iv) Convert the hexadecimal number 68BE to binary, and then convert it from binary to octal.

b) Represent the decimal number 5137 in 8 M

i) BCD, ii) excess-3 code

iii) 2421 code, and a 6311 code

3. a) Convert each of the following to the other canonical form:

i) $F(x,y,z)= \sum(2,4,5,6)$

ii) $F(A,B,C,D)=\pi(2,4,5,7)$

8 M

b) Draw a NAND logic diagram that implements the complement of the following function:

$F(A, B, C, D) = \sum (0, 1, 2, 3, 4, 8, 9, 10, 11, 12)$ 8 M

4. a) Implement full adder with a decoder. 8 M

b) Implement the following Boolean function using MUX

$F(A, B, C, D) = \sum (1, 3, 4, 11, 12, 13, 14, 15)$ 8 M

5. a) i) Explain basic configuration of combinational PLDs

ii) Design a combinational circuit using a ROM. The circuit accepts a three-bit number and outputs a binary number equal to the square of the input number.

8 M

b) Implement the following three Boolean functions with PLA:

$F1(A, B, C) = \sum (0, 1, 2, 4)$

$F2(A, B, C) = \sum (0, 5, 6, 7)$

$F3(A, B, C) = \sum (0, 3, 5, 7)$ 8 M

6. a) Explain D, SR, T and JK Flip-flops with logic diagram and function table. 8 M

b) Draw the circuit diagram and explain the operation of 4-bit universal shift register. 8 M